

REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-8, 15, and 17-22 are presently active. Claim 1 has been presently amended.

In the Office Action, Claims 1 and 7 were rejected under 35 U.S.C. § 103(a) as unpatentable over Karasawa et al (U.S. Patent No. 6,320,234) and Givens et al (U.S. Patent No. 6,080,655) in view of Applicant's Figure 22. Claims 2-6, 8, 15, and 17-22 were indicated as being allowed.

Firstly, Applicants acknowledge with appreciation the indication of allowance for Claims 2-6, 8, 15, and 17-22.

Secondly, regarding Claim 1, Claim 1 presently defines a second oxide film formed on *all upper surfaces* of the silicon nitride film. On the other hand, the structure closest to the present invention according to the Office Action is assumed to be the structure where a dielectric layer 52 (associated in the Office Action with the silicon nitride film of the present invention) and a barrier layer 30 (associated in the Office Action with the first oxide film of the present invention) disclosed in Fig. 3C of Givens et al for example are used for the interlayer dielectric layers 66 shown in Fig. 1 of Karasawa et al.

As the Office Action acknowledges, the dielectric layer 52 is used as an etching stopper, as shown in Fig. 3C of Givens et al.¹ Accordingly, a damascene line 74 is necessarily formed larger than a via 72. More specifically, the damascene line 74 is necessarily formed as a wiring layer on a part of the dielectric layer 52.

¹ Office Action, page 5, lines 12-13.

In the same manner, Karasawa et al show a structure where the diameter of a pad layer 90 is larger than that of an electrically conductive material 82. Therefore, even in the structure produced by a combination of Givens et al and Karasawa et al, because the pad layer 90 is necessarily formed on a part of the interlayer dielectric layers 66, it is impossible to form the interlayer dielectric layer 74 (associated in the Office Action with the second oxide film of the present invention) on all upper surfaces of the interlayer dielectric layers 66 (associated in the Office Action with the silicon nitride film of the present invention). Therefore, a structure of a second oxide film formed on *all upper surfaces* of the silicon nitride film, as defined in the amended Claim 1, cannot be obtained from the combination asserted in the Office Action.

Hence, for these reasons, it is respectfully submitted that Claim 1 and Claim 7 which depends from Claim 1 patentably define over the applied prior art.

This amendment is submitted in accordance with 37 C.F.R. §1.116 which after final rejection permits entering of amendments canceling claims, complying with any requirement of form expressly set forth in a previous Office Action, or presenting rejected claims in better form for consideration on appeal. The present amendment presents a minor change to Claim 1, thereby presenting rejected Claim 1 in better form for consideration on appeal. No new matter has been added, and this amendment does not raise new issues requiring further consideration and/or search. It is therefore respectfully requested that the present amendment be entered under 37 C.F.R. §1.116.

Finally, Applicants respectfully request that the Information Disclosure Statement filed December 6, 2000 (a courtesy copy of which is attached herewith with the date-stamped filing receipt) be initialed and returned with the next office action. Statements of Relevance

Application No. 09/729,816
Reply to Office Action of October 26, 2004

are available on the U.S. Patent and Trademark Office Patent Application and Information Retrieval System.

Consequently, in light of the above discussion, the present application as amended herewith is believed to be in condition for allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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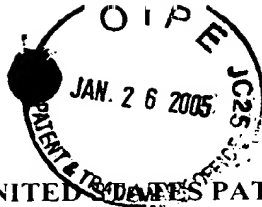
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GJM:RAR:clh

Attachment: Courtesy Copy of Information Disclosure Statement and PTO-1449 form filed
December 26, 2000, Date Stamped Filing Receipt

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Docket No. 200504US2



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Takuji MATSUMOTO, et al.

SERIAL NO: NEW APPLICATION

GAU:

FILED: Herewith

EXAMINER:

FOR: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

INFORMATION DISCLOSURE/RELATED CASE STATEMENT UNDER 37 CFR 1.97

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

COURTESY
COPY

SIR:

Applicant(s) wish to disclose the following information.

REFERENCES

- ☒ The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.
- ☐ A check is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

- ☒ Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the patent(s), together with a copy of the claims and drawings of the pending application(s) is attached along with PTO 1449.
- ☐ A check is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

- ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.
- ☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

- ☒ Please charge any additional fees for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



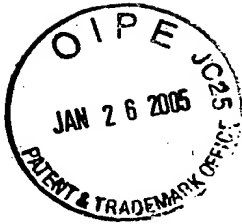
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LIST OF RELATED CASES

<u>Docket Number</u>	<u>Serial or Patent No.</u>	<u>Filing or Issue Date</u>	<u>Status or Patentee</u>
0057-2567-2YY	09/466,934	12/20/99	PENDING

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Form PTO 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 200504US2		SERIAL NO. NEW APPLICATION	
LIST OF REFERENCES CITED BY APPLICANT <div style="position: absolute; top: 50px; left: 100px; border: 2px solid black; border-radius: 50%; padding: 10px; text-align: center;"> OIPE JAN 26 2005 PATENT & TRADEMARK OFFICE </div>				APPLICANT Takuji MATSUMOTO, et al.			
				FILING DATE HEREWITH		GROUP	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL	AA	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA						
	AB						
	AC						
	AD						
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FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES NO		
	AO	58-124243	7/23/83	Japan (with English abstract)			X
	AP	11-87723	3/30/99	Japan (with English abstract)			X
	AQ	56-150853	11/21/81	Japan (with English abstract)			X
	AR	58-56450	4/4/83	Japan (with English abstract)			X
	AS	6-21373	1/28/94	Japan (with English abstract)			X
	AT	10-32266	2/3/98	Japan (with English abstract)			X
	AU	5-95116	4/16/93	Japan (with English abstract)			X
	AV	9-69610	3/11/97	Japan (with English abstract)			X
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
	AW	Y. Hirano, et al., "Bulk-Layout-Compatible 0.18µm SOI-CMOS Technology Using Body-Fixed Partial Trench Isolation (PTI)" 1999 IEEE, International SOI Conference, October 1999., (Pgs.131-132, 19-25)					
	AX	T. Matsumoto, et al., "Clarification of Floating-Body Effects on Current Drivability in Deep Sub-Quarter Micron Partially-Depleted SOI MOSFET's" Extended Abstracts of the 1999 International Conference on Solid State Devices and Material, Tokyo, 1999., (Pgs. 340-341)					
	AY						
	AZ						
Examiner					Date Considered		
*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

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OSMM&N File No. 200504US2

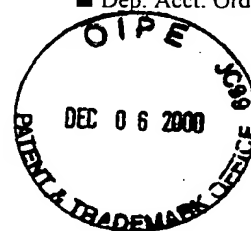
Serial No. NEW APPLICATION

In the matter of the Application of: Takuji MATSUMOTO, et al.

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING
THE SAME

The following has been received in the U.S. Patent Office on the date stamped hereon:

- ☒ 53 pp. Specification & 14 Claims/Drawings 14 Sheets (Formals)
 - ☒ Combined Declaration, Petition & Power of Attorney 4 pages
 - ☐ List of Inventor Names and Addresses
 - ☒ Utility Patent Application
 - ☒ Notice of Priority
 - ☒ Check for \$710.00
 - ☒ Fee Transmittal Form
 - ☐ Assignment/PTO 1595 pages:
 - ☐ Letter to Official Draftsman
 - ☐ Letter Requesting Approval of Drawing Changes
 - ☐ Drawings sheets ☐ Formal
 - ☐ Letter
 - ☐ Amendment
 - ☒ Information Disclosure Statement
 - ☒ Cited References (10)
 - ☐ Search Report
 - ☐ Statement of Relevancy
 - ☒ IDS/Related/List of Related Cases
 - ☐ Restriction Response
 - ☐ Rule 132 Declaration
 - ☐ Petition for Extension of Time
 - ☐ Notice of Appeal
 - ☐ Brief
 - ☐ Issue Fee Transmittal
 - ☒ White Advance Serial Number Card
 - ☐ Small Entity Status is Claimed
 - ☐
 - ☐
- ☐ CPA
 - ☒ Priority Doc (1)
 - ☒ Dep. Acct. Order Form
 - ☐ PTO-1449
 - ☒ Cited Pending Applications 1
 - ☐ Election Response



Due Date: 6/8/01

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